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In the Office Action mailed November 22, 2006, the Examiner rejected: (1) claims 1, 3, and 4 under 35 U.S.C. § 102(b); and (2) claims 2, 5, 6, and 32-35 under 35 U.S.C. § 103(a). Applicants have amended claims 1 and 3 to clarify that a buried oxide layer is located directly on a single surface of a polysilicon handle wafer or polycrystalline layer. No new matter has been added. Applicants submit that claims 1-6 and 32-35 are in condition for allowance and respectfully request notice to this effect.

I. Statement of the Substance of the Interview Conducted January 18, 2007

Participants of the interview included Examiner Pham and Applicants' representative Lisa Schoedel. No exhibits were shown nor demonstrations conducted. The participants discussed claim 1 as well as U.S. Patent No. 5,438,220 ("Nakagawa"). As a result of the interview, no agreement with respect to the claims was reached.

II. Response to the Rejection under 35 U.S.C. § 102(b) Based on "Nakagawa"

The Examiner rejected claims 1, 3, and 4 under 35 U.S.C. § 102(b) as being as being anticipated by Nakagawa. In claim 1, Applicants recite an RF semiconductor device. The RF semiconductor device includes three layers: a high resistivity polysilicon handle wafer, a buried oxide layer located directly on a single surface of the polysilicon handle wafer, and a silicon layer located directly on a surface of the buried oxide layer. Similarly, in claim 3, Applicants recite an RF

semiconductor device that includes three layers. However, in claim 3, the "polysilicon handle wafer" of claim 1 is replaced with a "polycrystalline layer."

The Examiner stated that Nakagawa's Fig. 18 teaches a semiconductor device comprising a high resistivity polysilicon handle wafer or polycrystalline layer 234, a buried oxide layer 2 located directly on the polysilicon handle wafer; and a silicon layer 4 located directly on the buried oxide layer. (Office Action, page 2.) Applicants respectfully disagree that Nakagawa's Fig. 18 teaches a buried oxide layer 2 located directly on the polysilicon handle wafer 234. Instead, Nakagawa's polycrystalline silicon film 234 is located within Nakagawa's oxide film 2 as seen below. However, Applicants have amended claims 1 and 3 to clarify that the buried oxide layer is located directly on a single surface of the polysilicon handle wafer or polycrystalline layer.

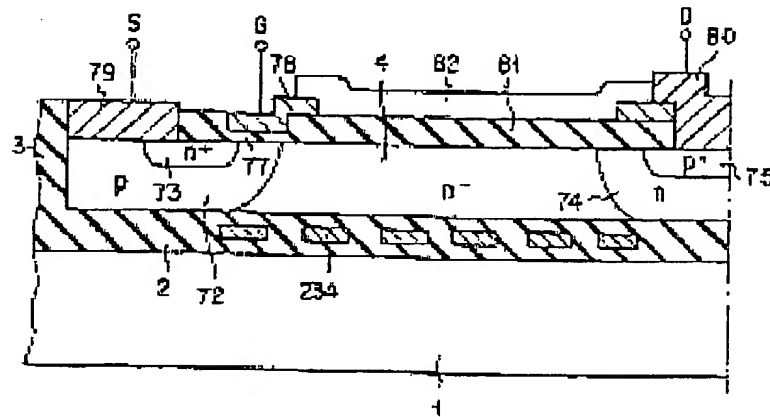


FIG. 18

Nakagawa does not suggest that the oxide film 2 is located directly on a single surface of the polycrystalline silicon film 234 because Nakagawa patterns the polycrystalline silicon film 234 in a strip or mesh form. (See, e.g., Nakagawa, col. 15, lines 13-16.) Because Nakagawa does not show or suggest a buried oxide layer located directly on a single surface of a polysilicon handle

wafer or polycrystalline layer, Applicants submit that Nakagawa does not anticipate claims 1 and 3. Claim 4 depends from claim 3. Accordingly, Applicants also submit that Nakagawa does not anticipate claim 4 for at least the reasons described above with reference to claim 3.

In light of the above, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 102(b).

III. Response to Claim Rejections under 35 U.S.C. § 103(a)

The Examiner rejected claims 2, 5, 6, and 32-35 under 35 U.S.C. § 103(a) as being unpatentable over Nakagawa in view of Applicants' Admitted Prior Art ("AAPA") and U.S. Patent No. 4,905,075 ("Temple"). Claims 2, 32, and 33 depend from claim 1. Claim 5-6, 34, and 35 depend from claim 3. As described above, Nakagawa does not show or suggest a buried oxide layer located directly on a single surface of a polysilicon handle wafer or polycrystalline layer. Neither AAPA, nor Temple overcomes the deficiencies in Nakagawa.

AAPA was cited for the teaching of using a high resistivity substrate to form RF devices. (Office Action, page 3). Temple was cited for the teaching of using a polysilicon wafer or handle having a resistivity of greater than 10^6 ohm-cm to provide a structure that can withstand mechanical shock. *Id.* Applicants respectfully disagree with the Examiner's interpretation of the teachings of AAPA. However, the Examiner's cited teachings of AAPA and Temple do not show or suggest a buried oxide layer located directly on a single surface of a polysilicon handle wafer or polycrystalline layer.

Because none of Nakagawa, AAPA, and Temple shows or suggests a buried oxide layer that is located directly on the polysilicon handle wafer or polycrystalline layer, the combination of

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Nakagawa, AAPA, and Temple does not show or suggest the claimed devices. Thus, Applicants submit that claims 2, 5, 6, and 32-35 are not obvious in light of the combination of Nakagawa, AAPA, and Temple.

In light of the above, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 103(a).


CONCLUSION

In light of the above amendments and remarks, Applicants submit that the present application is in condition for allowance and respectfully request notice to this effect. The Examiner is requested to contact Applicants' representative below if any questions arise or she may be of assistance to the Examiner.

Respectfully submitted,

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By:



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